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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,689	09/20/1999	ARMIN MRASEK	GR98P2610	1397

24131 7590 04/30/2004

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	19

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,689	MRASEK, ARMIN	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 15th of March 2004. Claims 1, 3 and 5 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 13th of November 2003. Currently, claims 1-6 are pending in this application.

Claim Objections

2. Claim 5 is objected to because of the following informalities:

In the preamble of the claim 5, substitute "controlled a microprocessor" by --controlled by a microprocessor-- in light of the original specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 5 and 6 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for reading out a number of data items by the microprocessor from the reception FIFO (See Application, page 13, lines 12-15), does not reasonably provide enablement for reading out data being currently written in the memory from the microprocessor (See Claim 5, lines 12-14). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. The Examiner doubts how to read out data, which is currently written in the memory, from the microprocessor in light of the specification. Actually, the Applicant discloses that the register RBC containing a number of data items to

be read by the microprocessor from the reception FIFO in the original specification, page 13, lines 12-15. The claim 6 is the dependent claim of the claim 5.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [hereinafter AAPA] in view of Ugajin et al. [US 5,046,039; hereinafter Ugajin].

Referring to claim 1, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled by a microprocessor (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data of a given data frame (See page 1, lines 7-10; i.e., wherein in fact that digital data is divided up into data frames of variable length implies said digital data of a given data frame) from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC Receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt signal (i.e., interrupt Int; See page 9, line 25) generated by a memory control unit (i.e., HDLC Receiver/ Transmitter), if said memory is full or if said memory contains an entry indicating an end of a respective data frame (See page 9, line 26 through page 10, line 1; i.e., wherein in fact that the HDLC Receiver always triggers an interrupt Int in the microprocessor if either the FIFO reception memory (viz., memory) is full or if the received D-channel signals (viz., a respective data frame) contain a byte indicating a frame end implies that informing said microprocessor, in a form of an interrupt signal generated by a memory control unit, if said memory (viz., FIFO reception memory) is full or if said memory contains an entry

indicating an end of a respective data frame (viz., a byte indicating a frame end of a respective data frame)); reading via said microprocessor said digital data from said memory (See page 2, lines 11-12; i.e., wherein in fact that a microprocessor removes the data contained in the FIFO memory implies that said microprocessor reads said digital data from said memory); and transmitting from said microprocessor to said memory control unit (i.e., HDLC Receiver/Transmitter) an acknowledgment of a reception of said data (viz., digital data) being read out from said memory (See Data signal and Ack signal from μP to HDLC Transmitter in Fig. 6A and B).

AAPA does not teach said memory having a settable size; determining via said microprocessor from said memory control unit a quantity of said digital data to be read from said memory; and setting via said microprocessor a size of said memory for a following writing procedure in said memory.

Ugajin discloses a buffer management system, wherein a memory (i.e., receiver buffer area 78b of Fig. 2) having a settable size (See col. 2, lines 1-12); determining (i.e., decision block in Fig. 3) via a microprocessor (i.e., means for executing software sequence of Fig. 3; See col. 3, lines 24-27 and col. 4, lines 4-8) from a memory control unit (i.e., LLC protocol unit 67 of Fig. 2) a quantity of digital data to be read from said memory (i.e., traffic flow of receiving data; See Fig. 5 and col. 4, lines 27-31); and setting (See block for "setting transmitter/receiver buffer length corresponding to initial value setting table" in Fig. 3) via said microprocessor (i.e., means for executing software sequence of Fig. 3) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area) for a following writing (i.e., receiving) procedure in said memory (See col. 4, lines 4-14; i.e., executing initial value setting for a following receiver buffering (viz., writing) operation in said receiver buffer area).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of managing reception buffer, as disclosed by Ugajin, in said method for transmitting digital data, as disclosed by AAPA, for the advantage of preventing the deterioration in

the communication performance by changing said memory size (i.e., receiver buffer area size; See Ugajin, col. 1, lines 8-14).

Referring to claim 2, AAPA teaches supplying said digital data from said first data bus (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) which checks whether said digital data has been received correctly (See page 1, line 25 through page 2, line 1 and lines 7-9; i.e., wherein in fact HDLC control device checks the data protection information implies that said HDLC logic unit checks whether said digital data has been received correctly) before said digital data is written to said memory (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC Receiver logic unit implies that said digital data (i.e., HDLC signal) has been received before said digital data is written to said memory).

7. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Ugajin [US 5,046,039] and Chee et al [US 5,673,416; hereinafter Chee].

Referring to claim 3, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to said first data bus (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC Receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC Receiver/ Transmitter), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line 1); and transmitting from said microprocessor to said memory control unit (i.e.,

HDLC Receiver/Transmitter) an acknowledgment of said data being written into said memory (See Data signal and Ack signal from μP to HDLC Receiver in Fig. 6A and B).

AAPA does not teach said memory having a settable size; and setting via said microprocessor a size of said memory for a following writing procedure in said memory.

Ugajin teaches a buffer management system, wherein a memory (i.e., receiver buffer area 78b of Fig. 2) having a settable size (See col. 2, lines 1-12); and setting (See block for "setting transmitter/receiver buffer length corresponding to initial value setting table" in Fig. 3) via said microprocessor (i.e., means for executing software sequence of Fig. 3) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area) for a following writing (i.e., receiving) procedure in said memory (See col. 4, lines 4-14; i.e., executing initial value setting for a following receiver buffering (viz., writing) operation in said receiver buffer area).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of managing reception buffer, as disclosed by Ugajin, in said method for transmitting digital data, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., receiver buffer area size; See Ugajin, col. 1, lines 8-14).

AAPA, as modified by Ugajin, does not teach performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data from said first data bus, and said microprocessor asking said memory control unit if said memory is ready to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory.

Chee discloses a memory request and control unit, wherein performing one of informing a microprocessor (i.e., display FIFO module 12 of Fig. 2), in a form of interrupt (i.e., DispDataAck from DRAM controller sequencer 22 to display FIFO module 12 in Fig. 3) generated by a memory control unit (i.e., DRAM

controller sequencer 22 of Fig. 3), if a memory (i.e., DRAM 24 of Fig. 3) is ready to accept new data (See col. 9, lines 20-23), and said microprocessor (i.e., display FIFO module) asking (i.e., a low priority request DispLoReq in Fig. 3) said memory control unit (i.e., DRAM controller sequencer) if said memory is ready to accept said new data. (See col. 10, lines 55-57); writing via said microprocessor said new data to said memory (See col. 9, lines 58-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of memory request and control unit, as disclosed by Chee, in said method, as disclosed by AAPA, as modified by Ugajin, for the advantage of utilizing simple circuit for said microprocessor (i.e., display FIFO module) for efficiently determining when to issue requests for said memory (i.e., DRAM access; See Chee, col. 2, lines 41-43).

Thus, AAPA, as modified by Ugajin and Chee, suggests placing said new data onto said second data bus (i.e., transmitting digital data (i.e., new data) to a second data bus; See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*).

Referring to claim 4, AAPA discloses supplying said new data (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) before it is placed onto the second data bus (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC Receiver logic unit implies that supplying said new data (i.e., HDLC signal) to a high-level data link control logic unit before it is placed onto the second data bus), said high-level data link control logic unit adding error-checking data (i.e., adding protection information) to said new data (See page 2, lines 16-18).

Response to Arguments

8. Applicant's arguments filed on 15th of March 2004 (hereinafter the Response) have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "the microprocessor sends a RFBS signal to the HDLC Receiver indicating 'a size of the memory for a following writing procedure in said memory' before the first Ack signal is sent from the microprocessor to the HDLC Receiver. Neither the RFBS signal nor the early Stat signal is present in AAPA (Fig. 6A & 6B)" on the Response page 9, lines 6-11, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that AAPA doesn't teach the above argued elements. However, the claim doesn't clearly recite the features upon which applicant relies (i.e., the microprocessor sends a RFBS signal to the HDLC Receiver indicating 'a size of the memory for a following writing procedure in said memory' before the first Ack signal being sent from the microprocessor to the HDLC Receiver). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, Ugajin teaches the claimed limitation, such that setting via said microprocessor (i.e., means for executing software sequence of Fig. 3) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area) for a following writing (i.e., receiving) procedure in said memory (See col. 4, lines 4-14; i.e., executing initial value setting for a following receiver buffering (viz., writing) operation in said receiver buffer area). After combining AAPA and Ugajin with rationale for the proper combination suggests all the limitations of the claim.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "'039 thereby pertains to variable partitioning of an intermediate memory between transmitting and receiving devices. Any such buffering or partitioning is NOT the object of the instant application." on the Response page 13, lines 11-14, the Examiner respectfully disagrees.

The Applicant essentially argues that Ugajin reference relied on in a rejection is inapplicable or cannot be combined because it does not related to solving the same problem that applicant is addressing in its

claimed invention (i.e., NOT the object of the claimed invention). The motivation to do what Applicant has done, however, does not have to be the same as the Applicant's to reach a conclusion of obviousness (See M.P.E.P. 2144). Moreover, the obviousness is not determined on the basis of purpose alone. *In re Graf,* 343 F.2d 774, 777, 145 USPQ 197, 199 (CCPA 1965). In summary, as long as there is some suggestion/motivation within the prior art to make the modification or combination, it does not have to be the same as the Applicant's.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Clearly, AAPA does not show 'setting via the microprocessor a size of the memory for a following writing procedure in said memory' as recited in claims 1 and 3 of the instant application." on the Response page 14, lines 13-16, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that AAPA doesn't teach the above argued elements. However, Ugajin teaches the claimed limitation, such that setting via said microprocessor (i.e., means for executing software sequence of Fig. 3) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area) for a following writing (i.e., receiving) procedure in said memory (See col. 4, lines 4-14; i.e., executing initial value setting for a following receiver buffering (viz., writing) operation in said receiver buffer area). After combining AAPA and Ugajin with rationale for the proper combination suggests all the limitations of the claim.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Although '416 does include a FIFO module, '416 not teach or suggest using HDLC data frames of variable lengths to transmit data from a first data bus to a second data bus operated asynchronously with respect to the first data bus." on the Response page 15, lines 2-6, the Examiner believes that the Applicant misinterprets the claim rejection.

The Applicant essentially argues that AAPA doesn't teach the above argued elements. However, the recited preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art, and therefore the argued element "using HDLC data frames of variable lengths to transmit data from a first data bus to a second data bus operated asynchronously with respect to the first data bus" is impliedly admitted to be old in the art by the Applicant. See MPEP 2129 *Admission as Prior Art.*
Thus, the Applicant's argument on this point is not persuasive.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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